New Phase-Lock Loop Circuit Providing Very Fast Acquisition Time

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Abstract—**We present a new circuit configuration for second-order phase-lock loops that provides, for large initial frequency offsets, acquisition times several orders of magnitude shorter than those achieved using conventional phase-lock loops. This new circuit also provides frequency locking almost instantaneously when the time delay around the loop is small. Furthermore, it can, without losing lock, sustain frequency changes several hundred times faster than those which can be sustained by a conventional circuit.**

I. Introduction

THE ACQUISITION TIME of a second-order phase-lock loop can be prohibitively long when the initial frequency offset $\Delta\omega$ between the input signal and the voltage-controlled oscillator (VCO) output signal is large compared to the loop natural frequency ω_n [1],[2]. Different techniques are employed to accelerate the acquisition time [3]–[5]. One commonly utilized technique uses a ramp-shaped periodic waveform to sweep the VCO frequency. With this scheme, the loop can acquire phase lock with certainty only if the VCO sweep rate is less than or equal to $4\Delta\omega/\omega_n^2$ [3]. This effect determines the minimum acquisition time. The scheme is complicated by the circuitry needed to generate the periodic ramp waveform and by the locking sensor for disabling the VCO frequency sweeping after acquisition. Two other methods are the combined frequency discriminator-phase detector scheme [4] and the dual-time-constant integrator scheme [5]. These acceleration techniques also need relatively complicated circuitry.

The acceleration method proposed in this paper requires a much simpler circuit than previous ones. This circuit is robust, easy to implement, and its performance is superior to that of prior techniques. Furthermore, it provides frequency locking almost instantaneously for loops having a small time delay. It also has a much greater capacity to remain locked against fast frequency changes.

To explain simply how the new result is obtained, we first review briefly the physical process responsible for the long acquisition time of a conventional second-order phase-lock loop. We then show how the circuit can be modified to speed up the acquisition process. The new circuit configuration is analyzed using numerical computations to obtain the phase error variation versus time. The acquisition time and the capture range are determined from these results. The analysis concludes with an evaluation of the circuit capacity to remain locked in the presence of rapid frequency changes and with the assessment of the influence of the damping factor. The last part of the study describes the experimental circuit and compares its results with those of a conventional second-order phase-lock loop.

Manuscript received February 7, 1985; revised April 15, 1985.
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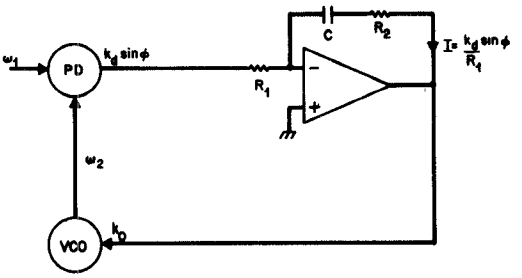

Fig. 1. Conventional second-order phase-lock loop using an active filter.

II. Conventional Phase-Lock Loop

Fig. 1 shows the schematic of a conventional second-order phase-lock loop in which an active filter integrates the error signal. The error signal between the input signal of angular frequency ω_1 and the VCO signal of angular frequency ω_2 is $k_d \sin\varphi(t)$. The quantity k_d depends on the amplitude of both signals and on the phase detector response. Its value is expressed in volts per radian. The quantity $\varphi(t)$ represents the phase difference between both signals.

The output of the integrator gives the control signal which tunes the VCO frequency according to the relation [1]–[2]

$$\frac{d\varphi}{dt} + k_0 k_d \frac{R_2}{R_1} \sin\varphi(t) + \frac{k_0 k_d}{CR_1} \int_0^t \sin\varphi(t)\,dt = \omega_2 - \omega_1. \tag{1}$$

The quantity k_0 is defined by the frequency–voltage relationship of the VCO control. Its dimension is expressed in rad/sec per volt. The quantity $\omega_2 - \omega_1$ is the initial frequency offset. The parameters k_d and k_0 combined with the resistances R_1 and R_2 and the capacitance C determine the natural loop frequency ω_n and the damping factor ζ according to the relations [1],[2]

$$\omega_n^2 = \frac{k_0 k_d}{CR_1} \tag{2}$$

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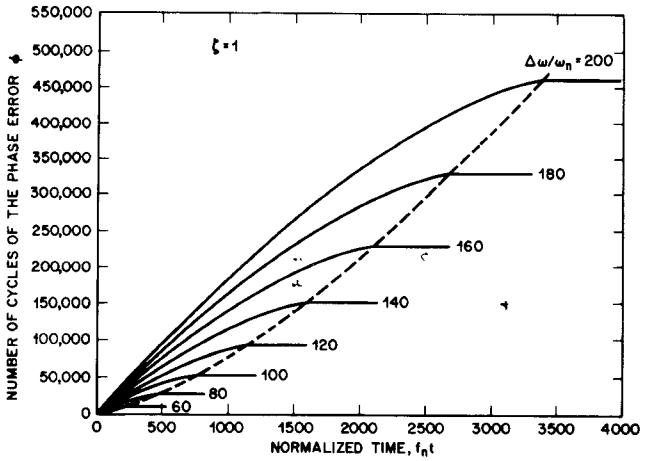


Fig. 2. Variation of the number of cycles of the error signal with normalized time before achieving phase-locking for a conventional second-order phase-lock loop. These results, obtained by computer simulations, are presented for increasing frequency offsets normalized relative to the loop natural frequency.

and

$$2\zeta\omega_n = k_0 k_d \frac{R_2}{R_1}. \tag{3}$$

Phase locking is achieved when the charge accumulated by the capacitance provides the bias voltage required to tune the VCO by $\omega_2 - \omega_1$, i.e., when

$$\frac{\omega_2 - \omega_1}{k_0} = \frac{k_d}{CR_1}\int_0^{t_l} \sin\varphi(t)\,dt. \tag{4}$$

The quantity t_l is the acquisition time. For large values of $(\omega_2 - \omega_1)/\omega_n$, it is given approximately by [1]

$$t_l \approx \frac{1}{2\zeta\omega_n}\left(\frac{\omega_2 - \omega_1}{\omega_n}\right)^2. \tag{5}$$

For example, a loop having a 200-Hz natural frequency and a damping factor of unity takes about 36 s to phase-lock when $(\omega_2 - \omega_1)/\omega_n = 300$.

The long duration of the acquisition process can be simply explained by noting that the biasing voltage developed across the capacitance C is obtained from the charge accumulated by the quasi-periodic current $k_d/R_1 \sin\varphi(t)$, whose period increases very slowly with time when $(\omega_2 - \omega_1)/\omega_n \gg 1$. The net charge accumulated per cycle of $\varphi(t)$, which is proportional to the area difference between the positive and the negative parts of the cycle, is correspondingly small. Therefore, it takes many such cycles to charge the capacitance to obtain the bias voltage required for phase-lock — several thousand in the previous example. This effect is illustrated in Fig. 2 for different values of the normalized initial frequency offset $(\omega_2 - \omega_1)/\omega_n$.

The reduction in the acquisition time is obtained in the proposed circuit by amplifying the error signal for values of $\varphi(t)$ close to $\pm\pi/2$, as explained in the following section.

III. New Phase-Lock Loop Configuration

The schematic of the new phase-lock loop circuit is shown in Fig. 3. It differs from the conventional loop by the addition of a circuit inserted between the phase detector and the integrator. This circuit consists of a network followed by an operational amplifier whose function is to provide an output voltage $V(\varphi)$ proportional to the current from the network. The network is made of a pair of antiparallel diodes shunted by a resistance R whose value is much smaller than the combined resistance of the diode pair when biased near zero voltage. The voltage $V(\varphi)$ is thus the sum of two terms; one is due to the current flowing through the resistance R; the other is caused by the diode current. Its value varies with the error signal $k'_d \sin\varphi$ as[1]

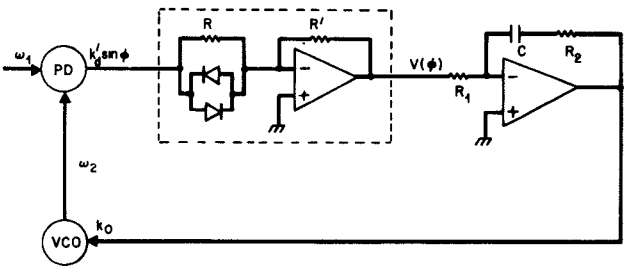


Fig. 3. New loop configuration.

$$V(\varphi) = R'\left\{\frac{1}{R}k'_d \sin\varphi + I_s \sinh\left(\alpha k'_d \sin\varphi\right)\right\}. \tag{6}$$

The quantities I_s and α are parameters characterizing the diode current variation with input signal [6]. The resistance R' determines the gain of the operational amplifier.

In the phase-locked state, the network current is mainly controlled by the resistance R because the fluctuations of φ are small around zero degrees and, thus, the combined diode resistance $(\alpha I_s)^{-1}$ is much larger than R. Consequently, $V(\varphi)$ can be expressed as

$$V(\varphi) \approx R'\left\{\frac{1}{R} + \alpha I_s\right\} k'_d \sin\varphi$$

$$\approx \frac{R'}{R} k'_d \sin\varphi. \tag{7}$$

To obtain the desired ω_n and ζ values as defined by (2) and (3), the resistance R' is adjusted to give

$$k_d = R'\left\{\frac{1}{R} + \alpha I_s\right\} k'_d$$

$$\approx \frac{R'}{R} k'_d. \tag{8}$$

As a result, the new loop configuration provides in the phase-locked state the same performance as the conventional loop having the same ω_n and ζ.

By contrast, the unlocked state resulting from an initial frequency offset gives rise to a network current controlled mainly by the diode pair when the phase error exceeds a given magnitude $|\varphi_0|$. This is achieved by adjusting k'_d to make $k'_d \sin\varphi_0$ large enough to drive the diodes into large current conduction. In this mode, a large surge of voltage is provided by the operational amplifier during the first cycle of the error signal. The surge can have a maximum value several hundred times larger than k_d, the maximum value

[1]For simplicity, $\varphi(t)$ is expressed as φ hereafter.

provided by the conventional loop. As a result, the time to charge the capacitance C is reduced. A more detailed analysis is given in the next section.

IV. Analysis

To satisfy the prior condition, we assume that R is adjusted relative to the low current diode resistance $(\alpha I_s)^{-1}$ so that 9/10 of the network current flows through R for small $|\varphi|$ values. Alternatively, the diode pair is driven into large conduction when the magnitude of the error signal equals about 0.6 V [6]. This implies a range of values for k'_d between about 0.7 V per radian and 2 V per radian, depending on the linear tracking range selected for φ. Consequently, the exponential factor $\alpha k'_d$ (hereafter designated as β) is between 6 and 30.[2] The voltage $V(\varphi)$ can thus be expressed simply as

$$V(\varphi) = k_d\left\{0.9\sin\varphi + \frac{0.1}{\beta}\sinh(\beta\sin\varphi)\right\}. \quad (9)$$

This voltage feeds the integrator and thus provides the control signal which tunes the VCO frequency. To obtain a more accurate expression relating the control signal to $d\varphi/dt$, we take into account the loop time delay τ, i.e., the time taken by the VCO to respond to the control signal. This effect, usually negligible in a conventional circuit, can give rise to phase error oscillations during acquisition caused by the rapid increase of $V(\varphi)$. To take this effect into account, we replace φ by φ' into (9) with

$$\varphi'(t) = \varphi(t-\tau). \quad (10)$$

The locking equation resulting from an initial frequency offset $\Delta\omega = \omega_2 - \omega_1$ is thus expressed as

$$\frac{d\varphi}{dt} + k_0k_d\frac{R_2}{R_1}\left\{0.9\sin\varphi' + \frac{0.1}{\beta}\sinh(\beta\sin\varphi')\right\} + \frac{k_0k_d}{CR_1}\int_0^t\left\{0.9\sin\varphi' + \frac{0.1}{\beta}\sinh(\beta\sin\varphi')\right\}dt = \Delta\omega. \quad (11)$$

The solution of this equation depends on the two loop parameters ω_n and ζ, on the diode exponential factor β, and on the initial frequency offset $\Delta\omega$. It can be normalized relative to ω_n by substituting $\omega_n t$ and $\omega_n\tau$ for the variables t and τ. In this case, the locking equation is expressed simply as (with $x = \omega_n t$)

$$\frac{d\varphi}{dx} + 2\zeta\left\{0.9\sin\varphi' + \frac{0.1}{\beta}\sinh(\beta\sin\varphi')\right\} + \int_0^x\left\{0.9\sin\varphi' + \frac{0.1}{\beta}\sinh(\beta\varphi')\right\}dx = \frac{\Delta\omega}{\omega_n}. \quad (12)$$

Numerical solutions of this equation are presented in the following sections.

V. Optimum Value of the Parameter β

To further the analysis, we determine the β values which yield the maximum (one-sided) normalized capture range $(\Delta\omega/\omega_n)_M$ for a given normalized delay $\omega_n\tau$. The results, obtained by computer calculations, are shown in Fig. 4 for the normalized delays $f_n\tau = 10^{-2}$, 10^{-3}, and 10^{-4}. The corresponding maximum normalized capture ranges are 20, 220, and 1900. They occur, respectively, for $\beta = 8$, 10.8, and 13.5. For the latter two values, there are phase oscillations during the first part of the phase acquisition process. The oscillations damp out after a short time interval, as illustrated by the results shown in Fig. 5, calculated for $\beta = 10.8$, $f_n\tau = 10^{-3}$, and $\Delta\omega/\omega_n = 200$. To minimize this effect, we select the near optimum β values of 8, 10, and 12 for, respectively, the normalized delays of 10^{-2}, 10^{-3}, and 10^{-4}.

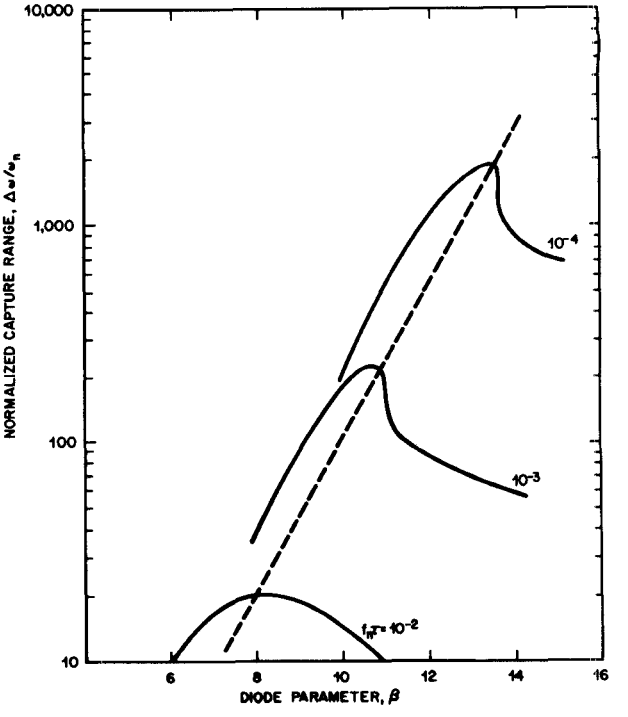


Fig. 4. Calculated maximum normalized capture range versus the parameter β for different normalized loop delays.

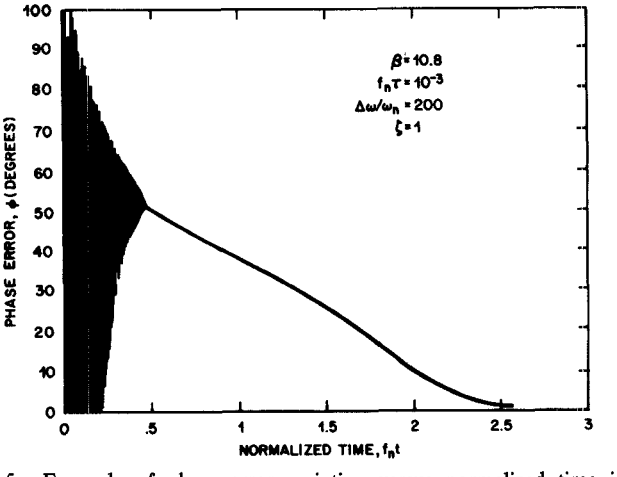


Fig. 5. Example of phase error variation versus normalized time in which there are significant initial phase oscillations due to loop delay.

VI. Variation of the Phase Error Versus Time

The variation of φ with $\omega_n t$ was calculated for $\zeta = 1$ and an initial phase error of zero. Figs. 6–8 show the results for the previously chosen β values of 8, 10, and 12 and the

[2] The diode parameter α^{-1} varies usually between 50 mV and 100 mV [6].

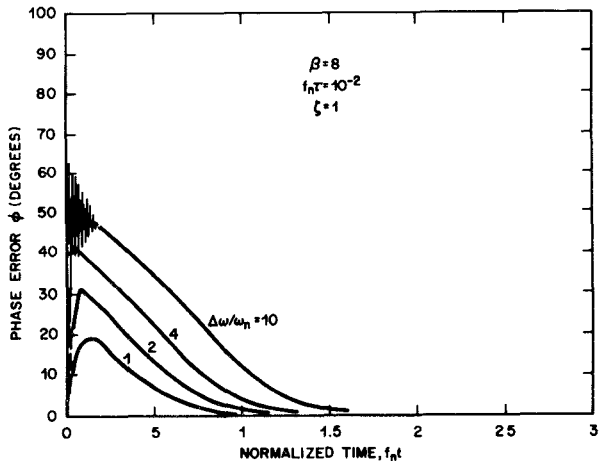


Fig. 6. Variation of the phase error versus normalized time calculated for the parameter values $\beta = 8$, $f_n\tau = 10^{-2}$ and $\zeta = 1$.

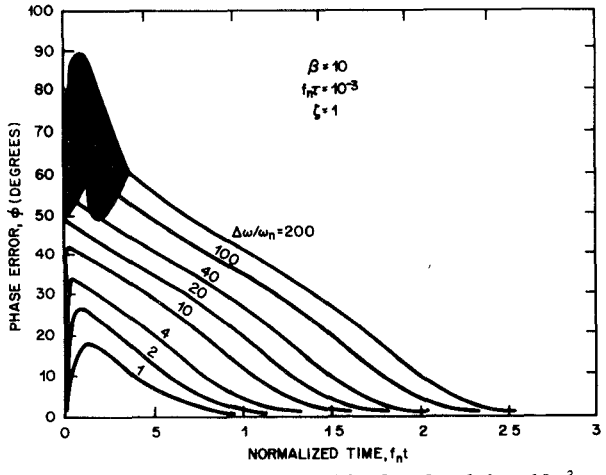


Fig. 7. Same results as in Fig. 6 for $\beta = 10$ and $f_n\tau = 10^{-3}$.

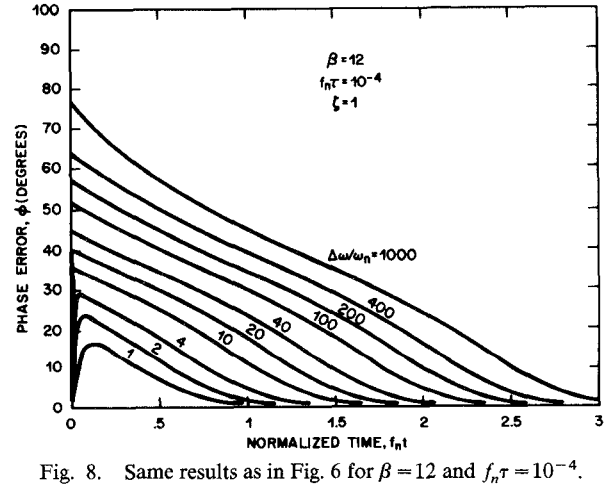


Fig. 8. Same results as in Fig. 6 for $\beta = 12$ and $f_n\tau = 10^{-4}$.

corresponding normalized delays $\omega_n\tau = 10^{-2}$, 10^{-3}, and 10^{-4}. The results are presented for a range of normalized frequency offsets $\Delta\omega/\omega_n$ varying from 1 to a value slightly below the maximum capture range achievable in each case. This choice avoids phase curves having large initial phase oscillations.

These results can be simply explained in the absence of phase oscillations as follows. Initially, φ increases almost linearly with $\Delta\omega t$. Concurrently, the current flowing in the feedback loop of the integrator increases as

$$\frac{k_d}{R_1}\left\{\frac{0.1}{\beta}\sinh(\beta\sin\varphi')\right\}$$

until the voltage developed across the resistance R_2 becomes equal to $\Delta\omega/k_0$; this is the voltage required to tune the VCO by $\Delta\omega$. When this happens

$$\Delta\omega/k_0 \approx k_d\frac{R_2}{R_1}\left\{\frac{0.1}{\beta}\sinh(\beta\sin\varphi_1)\right\}. \tag{13}$$

This occurs during the first cycle of the variation of φ for a phase error $|\varphi_1| \leq 90$ degrees, in the very short time interval

$$\Delta t \approx \frac{\varphi_1}{\Delta\omega}. \tag{14}$$

The time interval Δt is too short for any significant accumulation of charge into the capacitance C if $\Delta\omega \gg \omega_n$. At this time, $d\varphi/dt = 0$ and thus the VCO is frequency-locked with a phase error φ_1. This duration decreases in inverse proportion to $\Delta\omega$. For values $\Delta\omega/\omega_n > 10$, the corresponding variation of φ is compressed into the vertical axis as shown in Figs. 6–8 because Δt is too short for the time scale used in the graphs. For example, if $f_n = 1$ KHz and $\Delta\omega/\omega_n = 250$, the VCO is frequency-locked in less than 1 μs.

Thereafter, φ decreases to zero while the current flowing into the feedback loop of the integrator charges the capacitance C to give the final dc voltage required to keep the VCO frequency-tuned to ω_1. This happens after a duration t_l' defined by

$$\frac{\Delta\omega}{k_0} = \frac{k_d}{CR_1}\int_0^{t_l'}\left\{0.9\sin\varphi' + \frac{0.1}{\beta}\sinh(\beta\sin\varphi')\right\}dt. \tag{15}$$

VII. Acquisition Time Versus Initial Frequency Offset

We define the acquisition time as the normalized time f_nt needed for φ to decrease to one degree. The variation of the normalized acquisition time, designated as f_nt_l', versus $\Delta\omega/\omega_n$, is shown in Fig. 9 for the results given in the previous section. Its variation follows closely the relationship[3]

$$f_nt_l' \approx \frac{1}{\pi}\left\{\log_e\left(\frac{\Delta\omega}{\omega_n}\right)+2.8\right\}. \tag{16}$$

Note that the normalized acquisition time increases only by a factor of 3 as $\Delta\omega/\omega_n$ varies from 1 to 1000. In comparison, the normalized acquisition time required by the conventional loop having the same damping factor of unity varies according to Viterbi's expression as [1]

$$f_nt_l \approx \frac{1}{4\pi}\left(\frac{\Delta\omega}{\omega_n}\right)^2. \tag{17}$$

The acceleration provided by the new loop configuration is

[3] Expression (14) is obtained by curve fitting the numerical results.

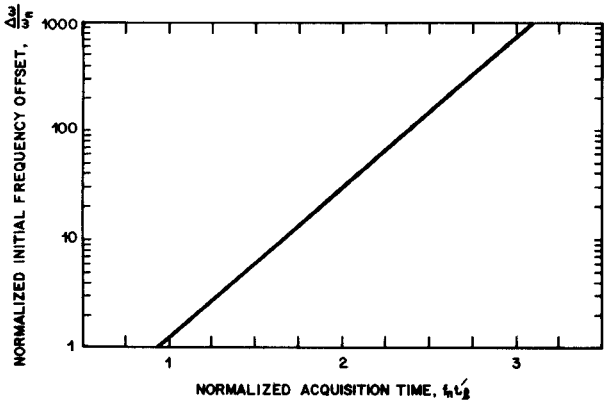


Fig. 9. Normalized initial frequency offset versus normalized acquisition time.

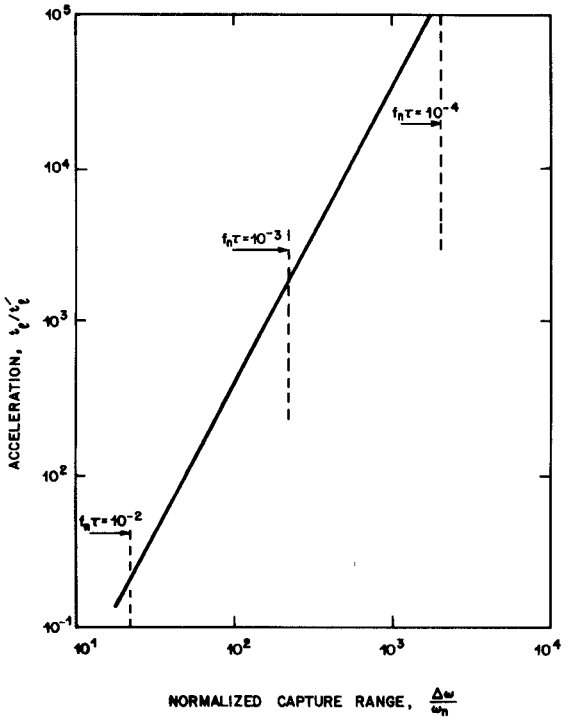


Fig. 10. Acceleration of the acquisition time provided by the new loop configuration relative to the conventional circuit versus the normalized capture range. Limits are presented for the three normalized loop delays $f_n\tau = 10^{-2}$, 10^{-3}, and 10^{-4}.

thus (for $\zeta = 1$)

$$t_l/t_l' \approx \frac{1}{4}\frac{(\Delta\omega/\omega_n)^2}{\log_e(\Delta\omega/\omega_n)+2.8}. \tag{18}$$

Fig. 10 shows the variation of (18) with $\Delta\omega/\omega_n$ (each dashed vertical line indicates the maximum capture range achievable for the corresponding value of $f_n\tau$).

VIII. Maximum Capture Range

The maximum normalized capture range depends on the parameter β whose optimum value is a function of the normalized delay $f_n\tau$, as illustrated in Fig. 4. Its value can be estimated by making $\varphi_1 = \pi/2$ in (13) yielding

$$\left(\frac{\Delta\omega}{\omega_n}\right)_M \approx \frac{2\zeta}{10\beta}\sinh(\beta). \tag{19}$$

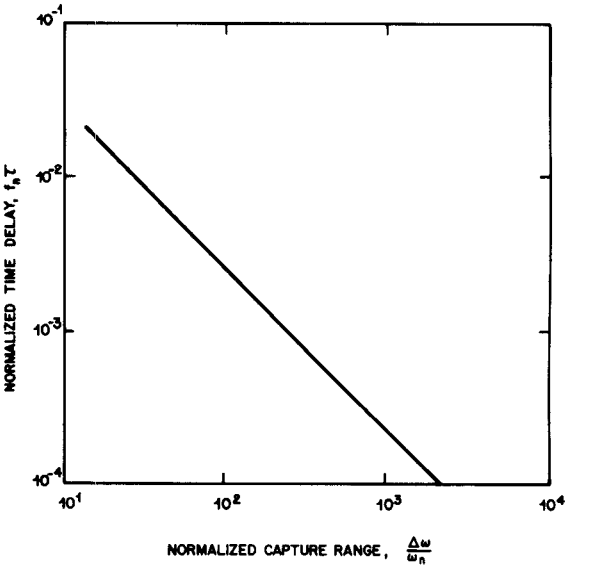


Fig. 11. Normalized loop delay versus normalized capture range.

For example, the near optimum values of $\beta = 8$, 10, and 12, corresponding respectively to the normalized delays of 10^{-2}, 10^{-3}, and 10^{-4}, yield in the case of $\zeta = 1$ the respective maximum normalized capture ranges of 37, 220, and 1329. In comparison, the computer calculations give for the same parameter values 35, 223, and 1356, respectively. In these results, φ varies less than one cycle. They can be increased slightly by letting φ skip a few cycles before locking. In this way, the normalized capture range can be increased for the previous set of $(\beta, f_n\tau)$ to 37, 246, and 1950, respectively, for a slight increase of the acquisition time. The quantity $(\Delta\omega/\omega_n)_M$ can also be expressed versus the normalized delay $f_n\tau$ from the results given in Fig. 4. Its variation is then given, as shown in Fig. 11, by the approximate relationship

$$\left(\frac{\Delta\omega}{\omega_n}\right)_M \approx \frac{2}{10}\frac{1}{f_n\tau}. \tag{20}$$

These results are valid as long as the operational amplifier used in the added nonlinear circuit is working in its linear range. The saturation of this amplifier, which usually occurs at ± 15 V, can reduce the capture range depending on the k_d values selected. The k_d value which gives rise to saturation is given by making $V(\varphi)_{\varphi=\pm\frac{\pi}{2}} = 15$ V in (9), yielding

$$k_{d_m} \approx \frac{15}{\frac{0.1}{\beta}\sinh(\beta)}. \tag{21}$$

If $k_d > k_{d_m}$, the capture range given by (19) is reduced by the ratio k_{d_m}/k_d.

IX. Capacity to Remain Locked in the Presence of Rapid Frequency Changes

The new phase-lock loop circuit also provides a much larger capacity to remain locked in presence of fast frequency changes. This effect can be seen by substituting

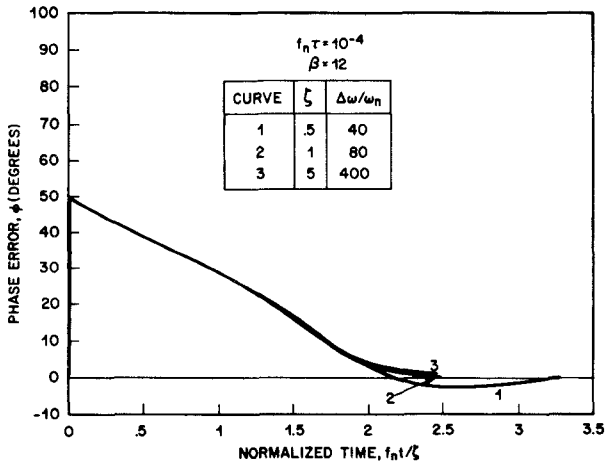


Fig. 12. Effect of damping factor on the variation of the phase error versus time normalized relative to loop frequency and damping factor.

into (12) a variable frequency offset $\Delta\omega(t)$. The maximum rate of frequency variation which can be sustained without losing lock is given by

$$\frac{d\Delta\omega}{dt} \approx \pm \omega_n^2 \frac{0.1}{\beta} \sinh(\beta). \tag{22}$$

In comparison, the conventional loop yields, in the same condition

$$\frac{d\Delta\omega}{dt} = \pm \omega_n^2. \tag{23}$$

The enhancement of the locking stability is thus

$$E_s \approx \frac{0.1}{\beta} \sinh(\beta). \tag{24}$$

For example, the new circuit can sustain a frequency change 678 times faster when $\beta = 12$.

X. Effect of the Damping Factor ζ

The effect of the damping factor ζ is illustrated by plotting the variation of the phase error φ with time, normalized by $f_n t/\zeta$. The variation thus obtained is almost the same for different values of ζ when the initial frequency offset is scaled by the parameter ζ. This effect is shown in Fig. 12, which gives the variation of φ versus $f_n t/\zeta$ for the three sets of values ($\zeta = 0.5$, $\Delta\omega/\omega_n = 40$), ($\zeta = 1$, $\Delta\omega/\omega_n = 80$), and ($\zeta = 5$, $\Delta\omega/\omega_n = 400$) for the case $\beta = 12$ and $f_n\tau = 10^{-4}$.

This result shows that the acquisition time increases proportionally with ζ. By contrast, the maximum capture range varies little for ζ varying from 1 to 5, and decreases with ζ when $\zeta < 1$. Therefore, the optimum value of the damping factor is close to one.

XI. Experimental Results

A. Circuit Configuration

An experimental circuit was built according to the schematic shown in Fig. 13 to verify the performance predicted by the computer calculations. The circuit has a dual configuration: one path provides a conventional second-order loop; the other path gives the new loop. This

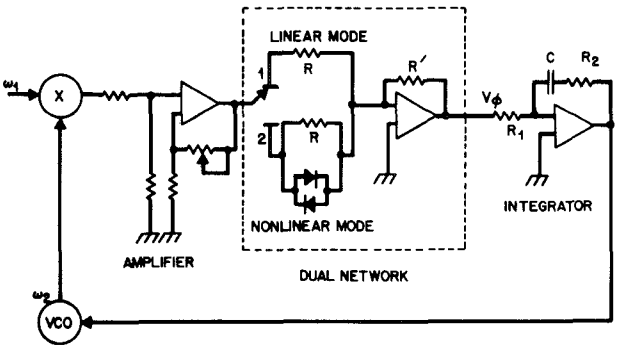


Fig. 13. Dual circuit used for measuring the acquisition time of a conventional circuit and that of the new configuration. Both circuits have the same small-signal natural frequency and damping factor respectively equal to about 168 Hz and 1.2.

dual configuration was selected to compare in a simple way the performance of both types of circuits.

The input signal was provided by a Hewlett-Packard synthesizer generator, model 3335A. The VCO was obtained using a Wavevek oscillator, model 114, having a voltage–frequency coefficient of 200 kHz/V around 1 MHz. The error signal was obtained using a double-balanced mixer giving an output voltage of 100 mV peak-to-peak.

The circuit contains three operational amplifiers. The first amplifier is used to raise the error signal to a peak value of about 0.6 V, as necessary to drive the diode pair into conduction in the presence of a frequency offset. It also provides a source of zero impedance to the second amplifier so that the resistance provided by the diode circuit does not effect the voltage gain.

The amplified error signal can be switched between two positions. Position 1 gives the conventional mode with a value of k_d adjusted to about 40 mV/rad. The adjustment of k_d is made by varying the operational gain R/R', with R equal to 200 KΩ. The new mode of operation is obtained by switching to Position 2, which directs the error signal toward another resistance R of 200 KΩ shunted by a diode pair whose combined small-signal resistance is several megaohms. Consequently, almost the same k_d value is obtained for the small phase error fluctuations of the locked state.

Finally, the signal is processed by a conventional active filter, consisting of an input resistance R_1 of 1 KΩ, and an operational amplifier having a feedback loop made of a damping resistance of 50 Ω in series with a capacitance of 45 μF. These values, combined with those of k_d and k_0 previously defined, yield a loop natural frequency of 168 Hz and a damping factor of about 1.2 for both modes of operation.

B. Acquisition Time Measurement

The acquisition time was measured for both modes of operation for the initial frequency offsets of ±30 KHz, ±60 KHz, and ±100 KHz. The measurements were made with a constant input signal frequency of 900 KHz and a variable VCO frequency. In the conventional mode, the

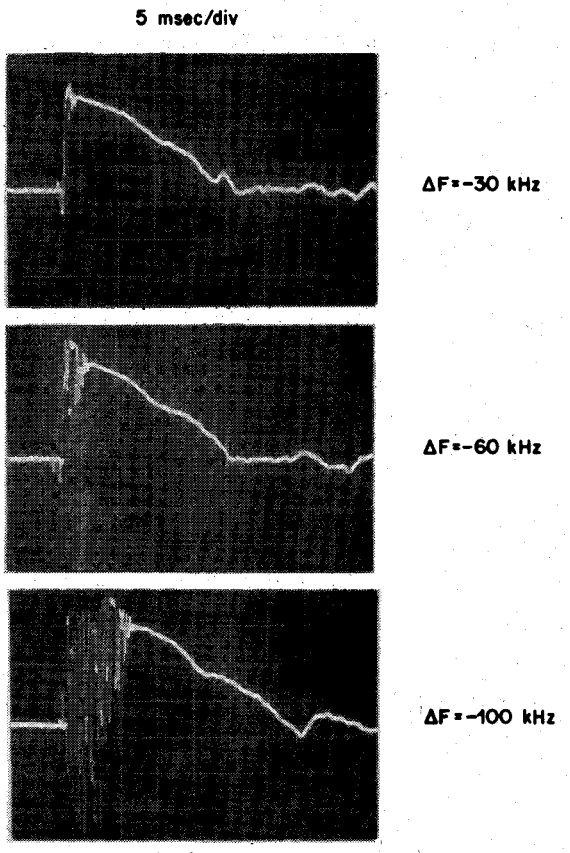


Fig. 14. Measured phase-error variation versus time for initial frequency offset of −30 KHz, −60 KHz, and −100 KHz from 900 KHz. The time scale is 5 ms/div.

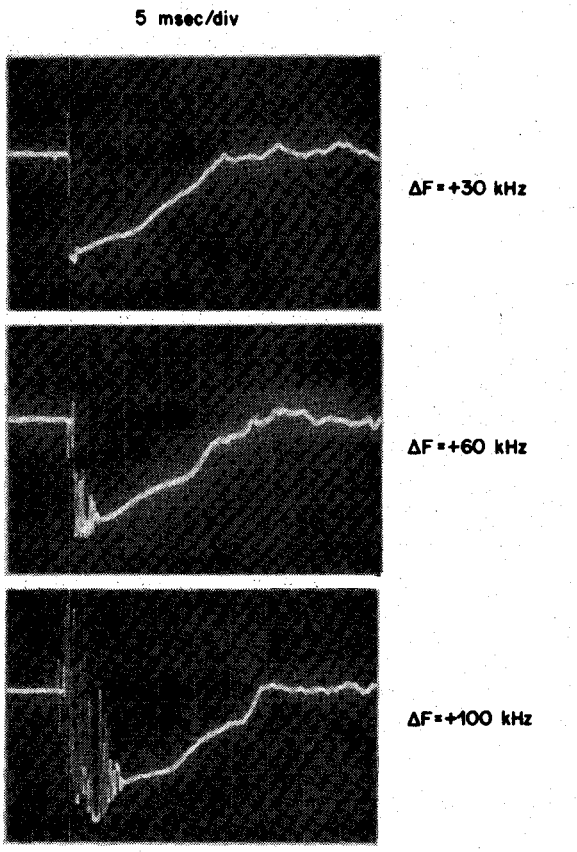


Fig. 15. Same results as in Fig. 14 for mutual frequency offsets of +30 KHz, +60 KHz, and +100 KHz.

corresponding acquisition times were 12 s, 48 s, and 190 s, respectively. In the new mode of operation, they were reduced, respectively, to about 20 ms, 22 ms, and 28 ms, as shown in Figs. 14 and 15, which show the variation of the error signal versus time. The acquisition time thus accelerated by about 600, 2000, and 6785, respectively. Table I summarizes these results.

The experimental results are found to be in good agreement with those predicted by numerical calculations. In particular, frequency locking is observed to be almost instantaneous for initial frequency offsets less than or equal to 30 KHz, as shown by the vertical rise of the phase error in Figs. 14 and 15. Larger frequency offsets give rise to initial phase oscillations caused by the loop delay. The magnitude and duration of the oscillations increase with the frequency offset, as predicted by the calculations. As expected, the acquisition time is found to increase very little with increasing frequency offsets. The negative and positive capture frequencies are, respectively, −120 KHz and 200 KHz, giving an absolute range of 320 KHz around 900 KHz. The asymmetry of the capture range is due to the variation of the frequency response of the phase detector.

TABLE I

$f_n \approx 168$ Hz $\zeta \approx 1.2$				
Δf (kHz)	$\Delta f/f_n$	t_ℓ (SECONDS)	t'_ℓ (MILLISECONDS)	t_ℓ/t'_ℓ
± 30	± 178	12	20	600
± 60	± 356	48	22	2182
±100	± 595	190	28	6785

C. *Locking Stability*

We also observed a much improved locking stability in the presence of fast frequency changes for the new mode of operation. The measurements were made by changing either the frequency of the VCO or that of the input signal. For example, the VCO frequency could be varied at a rate of several MHz/s without losing locking to the fixed input signal frequency. In comparison, the circuit switched to the conventional mode could only sustain a frequency variation of a few tens of KHz/s without unlocking. Similarly, the VCO was kept locked to an input signal whose frequency was varied in steps of 100 KHz from 700 KHz to 1300 KHz, each step changing in 1 ms. Such a result was unachievable in the conventional mode.

XII. Conclusion

We have shown that the acquisition time of a second-order phase-lock loop can be reduced by several orders of magnitude for initial frequency offsets large relative to the loop natural frequency. We have also shown that frequency locking can be made almost instantaneous within some limits imposed by the loop delay and the frequency offset. Furthermore, we have shown that the locking stability against fast frequency changes can be enhanced several hundredfold. These results are obtained by the addition of a very simple circuit to the conventional loop configuration.

Finally, we have given quantitative relationships for the effects of loop natural frequency and damping factor on capture range and acquisition time. Other important issues, such as performance in noise, have been addressed and will be reported in a separate paper.

Acknowledgment

The author is grateful to R. W. Wilson, L. J. Greenstein, and D. O. Reudink for helpful comments and suggestions on phase-lock loop operation. He also wishes to thank B. G. King and W. W. Snell for their assistance in the use of operational amplifiers and M. F. Wazowicz for helping to build the experimental circuit.

References

[1] A. J. Viterbi, *Principles of Coherent Communication*. New York: McGraw-Hill, 1966, chs. 2 and 3.

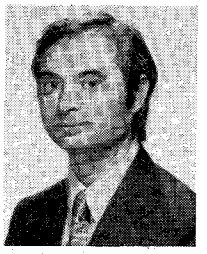
[2] F. M. Gardner, *Phaselock Techniques*. New York: John Wiley, 1966, ch. 1.

[3] J. J. Spilker, *Digital Communications by Satellite*. Englewood Cliffs, NJ: Prentice-Hall, 1977, ch. 12.

[4] P. S. Henry, "Frequency agile millimeter-wave phase-lock system," *Rev. Sci. Instrum.*, vol. 47, no. 9, pp. 1020–1025, Sept. 1976.

[5] D. Richman, "The dc quadricorrelator: A two-mode synchronization system," *Proc. IRE*, pp. 288–299, Jan. 1954.

[6] M. V. Schneider, "Electrical characteristic of metal-semiconductor junction," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-28, pp. 116–117, Nov. 1980.



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